AN1531

Parameter Extraction Techniques for RF Power Transistor Models

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Today's RF circuit designer has many circuit response simulation models at his disposal to speed breadboarding, and to provide some unique analysis capabilities. Some of these models employ rigorous transistor models based to a large extent upon the Integral Charge–Control bipolar transistor model published by H. K. Gummel and H. C. Poon in 1970.(1) The G–P model basically improves upon the DC model of Ebers and Moll(2) in that it incorporates parasitic resistances, capacitances, high injection effects, transit times, and bias dependencies.

Our major concern here is with the accuracy and physicality of the model parameters, as evidenced by the precision of the circuit simulation. Since parameter extraction from DC and AC measurements involves curve fitting and extrapolation from tangents, one must take care to arrive at solutions that are physically rational as well as satisfying the requirements for a good fit.

All parameters are extracted from DC and AC measurements which can be taken on equipment such as depicted in Figure 1. Note that in some cases the scalability of SPICE(3) parameters was employed by taking measurements on devices fabricated specifically for the analysis by using a single building block while the actual amplifier transistor was composed of twelve of these blocks.

It should be pointed out that we are working backwards from a fully characterized 900 MHz, class C amplifier, as well as forwards from the device measurements to verify how closely the G–P model simulates the amplifier performance and therefore, how useful a tool SPICE might be to predict the performance of future designs. We are also interested in the optimization of the transistor design insofar as how SPICE indicates we should play the design tradeoffs.

We begin with those parameters derived from DC measurements.

PARAMETER EXTRACTION FROM DC MEASUREMENTS

The most informative DC measurement to be performed is known as the "Gummel Plot" (Figure 2). This is simply a log vs. linear plot of collector and base currents (I_C and I_B) vs. the intrinsic base–emitter forward bias voltage ($V_{B'E'}$) with V_{BC} = 0. From this plot one can determine:

the transport saturation current (I_S),

ideal maximum forward beta (B_F),

the forward current emission coefficient (N_F),

the base–emitter forward bias leakage emission coefficient (N_E),

the base–emitter forward bias leakage saturation current (I_{SE} or C_2),

the forward knee current (I_{KF}).

Transport Saturation Current (I_S) is obtained by extrapolating the plot of the natural log of collector current to the y axis (V_{BE} = 0). I_S is a fundamental parameter whose extraction is perhaps the most obvious and accurate. The value obtained for I_S is proportional to the area of the emitter base junction, and therefore is device type dependent.

Ideal maximum forward beta (B_F) can be determined from the maximum separation between the two curves (I_C/I_B), and varies substantially from wafer lot to wafer lot. A typical low noise transistor may have B_F from 100 to 200, while a 12.5 volt, class C power transistor will typically have a B_F of 40 to 80.

The forward emission coefficient (N_F) is extracted from the slope of the I_B locus in the mid region of the plot (where it is parallel to the I_C locus, i.e., the region of constant Beta) and models the deviation from ideal slope. N_F typically has a value of close to 1.0 for an RF transistor.

The base–emitter low level forward bias emission coefficient (N_E or n_{EL}) is typically 1.0 to 2.0 for a shallow junction transistor (when in doubt, use 1.5), and is extracted from the slope of the I_B line near the Y axis and defines its deviation from ideality:

$$\text{Slope} = q/(NE)KT$$

The base–emitter leakage saturation current (I_{SE}, or for older versions of SPICE, C_2) models leakage current of the forward biased base–emitter junction. It is obtained from the Y axis intercept of the extrapolated curve for IB.

$$(\text{Y intercept}) = C_2 I_S$$

Forward knee current (I_{KF}) characterizes the onset of high injection effects, and is the point where the slope of the I_C curve changes to half its original value. In the expression for I_C in the Gummel–Poon model, I_{KF} has a profound effect upon simulations in the high current regime. Using a value

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of 10 to 20 times the extracted parameter relieves the sensitivity of the model to other parameters, particularly V_{AF} and V_{AR}. Some analysts believe a second model should be developed for high current application. It is a fact that the Gummel–Poon model for H_{FE} roll–off with current is consistently more gradual than is physically observed. For a class C amplifier simulation where both high current and high voltage excursions occur, a compromise clearly must be made.

Similarly, a group of parameters is extracted from the Gummel Plot of the reverse transistor (i.e., exchanging collector for emitter) (Figure 3), yielding:

maximum reverse beta (B_R),

reverse current emission coefficient (N_R),

base–collector leakage emission coefficient (N_C),

base–collector saturation current (I_{SC} or C_4),

and reverse knee current (I_{KR}).

Since an RF power transistor is seldom used in the reverse mode, these parameters can be allowed to default without significant degradation to the model.

Extracted from DC Beta plots (I_C vs V_{CE} for stepped I_B) are measurements from which the forward Early Voltage (V_{AF}), and collector resistance (R_C) can be extracted.

V_{AF} can be graphically determined (Figure 4) by extending a tangent of the I_C plot to intercept the X axis (a negative number). The forward Early Voltage is an indication of the doping level of the active base in the vicinity of the collector. As the voltage across the collector–base junction is increased, the effective base charge is reduced as the junction depletion area spreads into the base, and so forward beta increases (the Early Effect[3]). The Gummel–Poon model uses this effect to model variation in base charge, so that as the device approaches high current saturation, the parameter's effect becomes pronounced.

For lower frequency devices with deeper bases (f_t < 2 GHz), V_{AF} is typically over 100 volts, but for very high frequency NPNs, and especially PNPs, the Early Voltage may be considerably less than 50 volts. (When making measurements of Early voltages, it is important to keep the device out of breakdown effects which are largely responsible for the non–parafocality of tangents.) We have had our best results using low current, low voltage regions for the measurements.

R_C can be extracted as $R_{C(sat)}$ and/or $R_{C(active)}$ by calculating the slope of the line tangent to the I_C curve in the saturation region, or through the knees of the active region, respectively (Figure 5).

$R_{C(sat)}$ can also be determined from the "flyback measurement" generally used to measure R_E[4]. This is simply the plot of collector to emitter offset voltage vs base current while the collector current is held to a minimum (Figure 6). Practically speaking, a DVM across the collector and emitter terminals while forcing 10 or 100 mA base current will yield the series emitter resistance. A curve tracer will give a display of the plot showing the negative resistance characteristic at low currents, hence the term "flyback measurement." The collector saturation resistance can be determined by allowing a small amount of collector current to flow and noting the change in apparent resistance for the change in current.

The reverse Early Voltage (V_{AR}) is similarly extracted from the reverse beta plot (Figure 7). Because the reverse transistor's "collector" is the heavily doped emitter region of the forward transistor, the junction depletion area spreads more readily into the lightly doped base, and V_{AR} is consequently much less than V_{AF}.

At this point it is worthwhile to observe the accuracy of the DC parameter extractions with a simulation vs. measured data overlay using a forward characteristic such as the Gummel Plot (Figure 8) or H_{FE} vs. I_C plot (Figure 9). It is likely that the fit will be poorest in the high current regime. Optimization can be performed to try for a better fit. I_{KF} is the parameter to change (increase) to get results which will yield a model most consistent with RF amplifier performance. (It is not unusual for a manufacturer to specify an I_{KF} for a device which is 10 times the maximum collector current rating.) Base current simulation will be improved when the parameters for R_B, R_{BM} and I_{RB} are included, but base resistance is not accurately measured with a DC test.

PARAMETER EXTRACTION FROM CAPACITANCE vs. VOLTAGE MEASUREMENTS

Capacitance parameters are obtained by employing curve fitting techniques, assuming that capacitance vs. voltage follows the model:

$$C_j(V) = C_jO / (1 - V / f)^m + C_{(para)}$$

$C_{(para)}$, the parasitic capacitance of the package, bond pads, and die metallization must be measured and/or calculated. With the appropriate algorithm, $C_{(para)}$ can also be curve fitted. A reasonable approximation of $C_{(para)}$ would be 20% of specified capacitance at rated voltage for a typical 12 volt UHF transistor, to over 50% for a 50 volt microwave pulsed power transistor.

Barrier potential f is typically 0.5 to 0.7 volt. The gradient factor m is expected to be .33 to .50, representing the graded junction and abrupt junction respectively (an emitter base junction is typically abrupt while the collector base junction is typically somewhere between abrupt and graded). Specific conditions such as collector substrate grading can lead to effective values of m beyond the normal range. More rigorous models are needed.

Simulation programs such as SPICE use f and m only to calculate capacitance vs voltage, so even though the absolute numbers arrived at through curve fitting may not be physical, the circuit simulation results may be good. The art is to set limits for parameters derived from device layout and process knowledge, and force the optimization of the curve fit (Figures 10, 11).

An additional parameter, F_C, is included to model the slope of the CV curve in the forward biased region. 1.0 is a typical value found for F_C.

PARAMETER EXTRACTION FROM AC MEASUREMENTS

Forward transit time (t_F) is the sum of the emitter to collector time delays for carrier propagation through a transistor, and can be determined from the measurement of h_{fe} over a range of frequencies and collector currents. The common emitter forward current gain is most easily derived for RF and microwave devices by first measuring the scattering parameters on a network analyzer, and then converting to the hybrid parameters. There are now a number of network analyzer systems available offering semi–automatic, and automatic parameter extraction and

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calibration. Many systems offer on–line conversion from 'S' parameters to other parameters including 'h' parameters. Determination of transit time from h_{fe} then becomes a relatively simple task of plotting the inverse product of the forward current gain (h_{fe}) and radian frequency ($1/2\ \pi f_t$) vs. the reciprocal of collector current. For devices without a well defined constant region, the intercept on the ($1/2\ \pi f_t$) axis of a line tangential to the slope determines the ideal transit time (Figure 12).

Bias dependence of the transit time is modeled by three additional factors:

coefficient for bias dependence (X_{tF})

high current parameter for effect on transit time (I_{tF})

Voltage describing Vbc dependence on transit time (V_{tF}).

These factors model the high current roll off of f_t, and the decrease in collector transit time with increasing collector–base voltage.

Transit time including these bias corrections becomes:

$$t_{FF} = t_F\ (1 + X_{TF}\ (I_F / (I_F + I_{tF}))2e^{(Vb'c')/(1.44V_{tF})}$$

$$I_F = I_S\ (e((qVb'e') / (NF*kt))$$

The coefficient for bias dependence, X_{tF}, and the high current parameter, I_{tF}, are determined from the best curve fit that approximates the roll off of f_t at high currents at the desired operating voltage. The voltage dependence is similarly determined by varying the collector voltage at a collector current higher than that corresponding to the minimum transit time, and determining a value for the voltage dependence factor that gives the optimum fit to the measured data.

The total reverse transit time can be measured on a network analyzer by the same method, but with the transistor operating in the inverted mode (Figure 13). This works reasonably well if the reverse beta is significantly higher than 1. If this is not the case, then it can be computed from the saturation delay time constant, t_{sat}, which defines how long the transistor takes to dissipate the excess base charge after operating in saturation.

These parameters are related by[6]:

$$t_{RL} = t_{sat}\ (1 – (\partial f/\partial r)\partial r – (\partial f/\partial r)t_f$$

Base resistance, (R_b), is the total resistance influencing base current. It has three component parts (Figure 14): the resistance of the intrinsic base under the emitter ($r_{bb'}$), the extrinsic base resistance between the emitter periphery and the base contact ($r_{b'}$), and the base contact resistance (r_{bcon}).

Extrinsic base resistance is normally minimized by heavily doping the base region under the ohmic contact. The extrinsic base resistance is given by

$$r_b = (p / (2L_{em}X_{jb}))$$

where L_{em} is the total length of the emitter fingers, p is the average resistivity in the emitter–base spacing region of separation and X_{jb} is the depth of the extrinsic base region.

The intrinsic base resistance $r_{bb'}$ is given by

$$r_{bb'} = p_{bb'} / (2n * W_bL_{em})$$

where $p_{bb'}$ is the average resistivity of the base under the emitter and W_b is the base width under the emitter. The factor n is a function of emitter current and defines the bias dependence of the base resistance. This is a result of current crowding to the emitter periphery with increasing emitter current and conductivity modulation of the intrinsic base caused by injected carriers. At low currents n = 1, increasing to n > 3 at normal currents.

Because of the distributed nature of the base resistance, it is difficult to accurately measure. Base resistance can be approximately determined by a number of methods, and the choice of the most appropriate depends on the final application[7]. R_b can be determined by dc methods, for example from the log $I_b/V_{b'e'}$ characteristic, but these methods have proven inaccurate for large power transistors. One method that can be used on VHF/UHF bipolar transistors, is the determination of R_b from the input impedance circles. The locus of input impedance, h_{ie}, plotted over a wide range of frequencies, describes a semicircle (Figure 15) which intercepts the real axis at both dc and at high frequency. Neglecting the effects of parasitic and collector depletion capacitance, the high frequency intercept is given by[8]:

$$RE\ (h_{ie}) = r_{bcon} + r_{b'} + r_{bb'} + r_{e'} + w_tL_e$$

The effect of the parasitic capacitances, C_{bc} and C_{be}, and the extrinsic collector junction capacitance, C_o, is to reduce the real component of h_{ie} by an amount depending on the magnitude of h_{ie}. Including this capacitance, and, as h_{in} approaches the real axis, at high frequency the real part of the input impedance can be approximated by[9]:

$$RE\ (h_{in}) = RE\ (h_{ie}) / (1 + B^2 * RE\ (h_{ie})^2)$$

where

$$B = 2\pi \geq f\ (C_{bc} + C_{be} + C_o)$$

Accurate determination of R_b by this method depends on a knowledge of the emitter inductance, and the parasitic package and transistor capacitances. For transistors with high f_t, small values of base resistance are easily swamped by the dominant emitter inductance term.

Difficulties in measuring the 'h' parameters at high frequencies are best avoided by the more practical method of measuring the 's' parameters. The base resistance is a function of the current, and this dependence is modeled in the circuit simulator by allocating a low and high current value for the base resistance, R_B and R_{BM}, and a current at which R_B falls half way to the minimum value, I_{RB}. Input impedance circles are required over a range of bias currents to determine these values.

Calculating the base resistance from the geometry of our test device, using the equations given earlier, shows good agreement with the extracted low current value (2.7 ohms and 2.6 ohms respectively). The calculated high current value of 1.22 ohms is approximately twice the measured value. This calculation does not, however, account for the base–emitter capacitance shunting the base current at high frequencies. Because of this, more current is crowded into the emitter periphery thus further decreasing the effective base resistance under the emitter.

For class 'B' and 'C' amplifier simulations, R_b can be represented by the high current value without much loss of accuracy.

APPLICATION OF SPICE IN CLASS 'C' AMPLIFIER DESIGN

Parameters determined by the above methods can be used to simulate the operation of class 'C' amplifier circuits and gain an appreciation of the various terminal current and voltage waveforms. SPICE has been used to simulate an

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rf transistor operating as a class ‘C’ amplifier at 870 MHz with 12.5 volt collector bias, with the results compared to the performance of an actual circuit.

The 12 cell interdigitated geometry used in this comparison was packaged in a UHF flange package, with double emitter wire bonds to minimize package inductance. Some SPICE parameters were extracted on a single cell die to improve accuracy. These parameters were then scaled for a larger die. At an output power of 5 Watts, measurements were made of the input and output impedances at the fundamental, second and third harmonics. Impedance transforming networks on input and output were modeled to accurately represent the load seen by the transistor (Figure 16). Since the performance, especially efficiency, is strongly dependent on the collector harmonic loading, operating conditions of the best amplifier were replicated as closely as possible. In a synthesis role the packaged transistor impedances would normally be calculated from the terminal current and voltage waveforms. SPICE was able to predict the gain within 0.5 dB of the performance of the actual circuit.

Collector voltage for the initial 100 nsec after the start of the analysis is shown in Figure 17. Because the operation of the circuit is highly non–linear, and certain of the circuit time constants are relatively long, a number of cycles need to be analyzed before the response reaches a quasi–static solution. The collector voltage waveform indicates a damped oscillation exists, eventually decaying after approximately 150 nsec. The oscillation is a resonance of the collector bias choke with the collector capacitance, and illustrates the need for long analysis periods.

Five cycles have been expanded in the subsequent plots to show the collector and base voltage and current waveforms (Figures 18, 19). The collector and base current waveforms are forced to be sinusoidal by the active matching networks. SPICE also provides the facility for determining the circuit performance as a function of frequency, but only for small signal conditions, and therefore is unusable when the device is initially biased off.

Although SPICE does not provide circuit optimization capabilities, when allied with network synthesis and analysis programs (i.e. SUPERCOMPACT[10] or TOUCHSTONE[11]) circuit performance can be evaluated and the design checked to ensure maximum ratings are not exceeded. The effects of changes in the device parameters can also be assessed and the influence of parasitic components can be analyzed. This is demonstrated by the influence on gain and collector efficiency of emitter inductance variations shown in Figure 20.

CONCLUSIONS

While linear models for RF circuit response have been in use for some time, models based upon intrinsic transistor parameters have only recently found utility in predicting RF power amplifier response. Extraction of these parameters from I–V, C–V and AC measurements is still, however, something of an art. Utilizing these models to characterize the AC response of a class C amplifier gives insight into device design and process optimization, as well as circuit performance considerations.

To demonstrate this approach to computer aided design, a 12.5 Volt, 870 MHz, 5 Watt, class ‘C’ amplifier has been modeled, and the results discussed, especially model parameter extraction.

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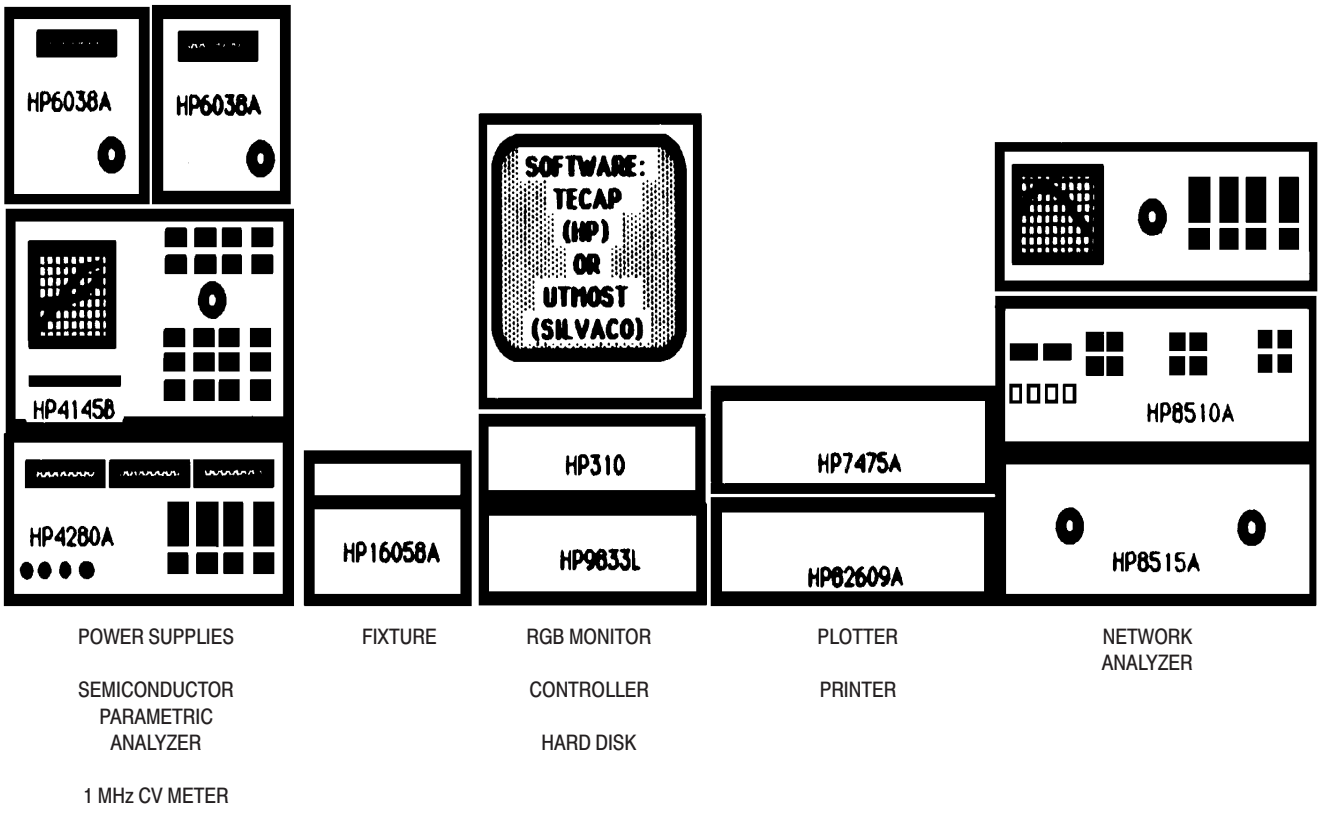

Figure 1. Parameter Extraction Hardware

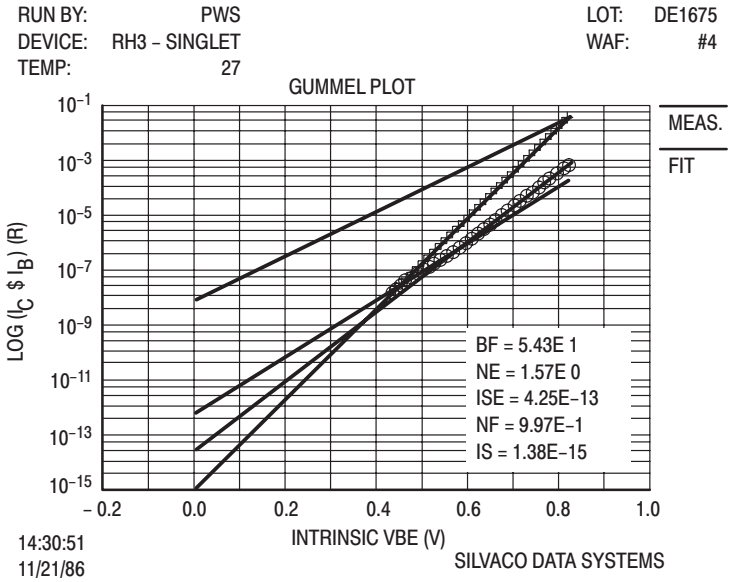

Figure 2. Gummel Plot

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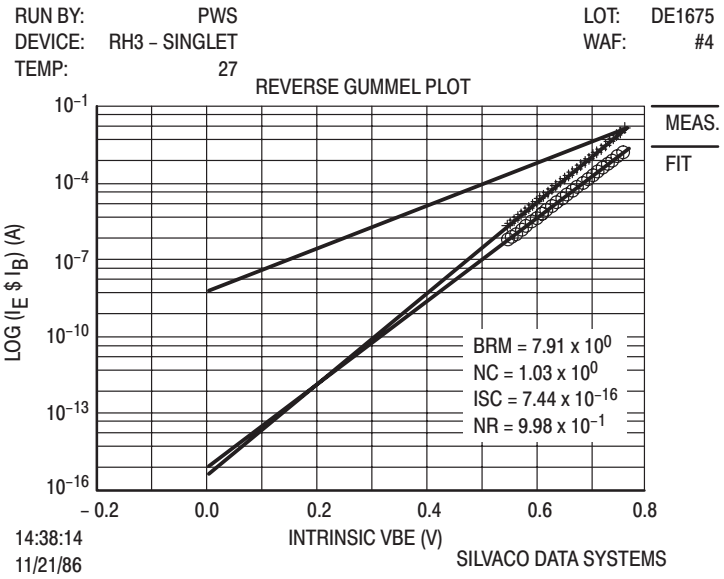

Figure 3. Reverse Gummel Plot

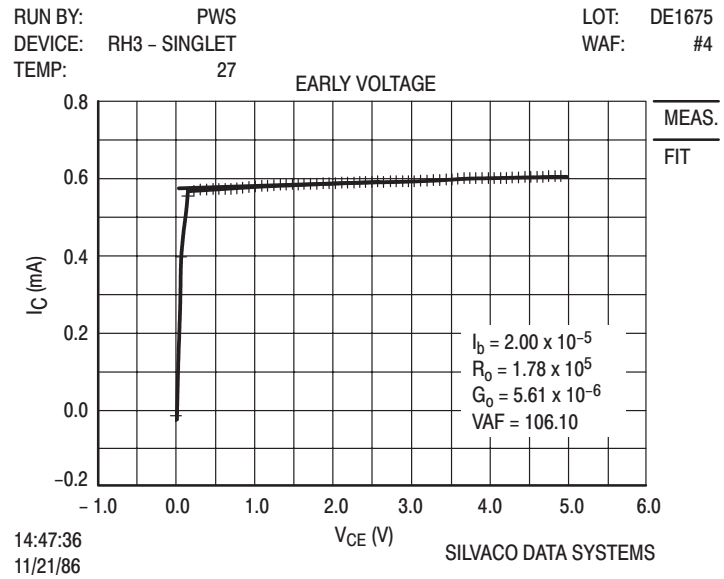

Figure 4. Forward Early Voltage Plot

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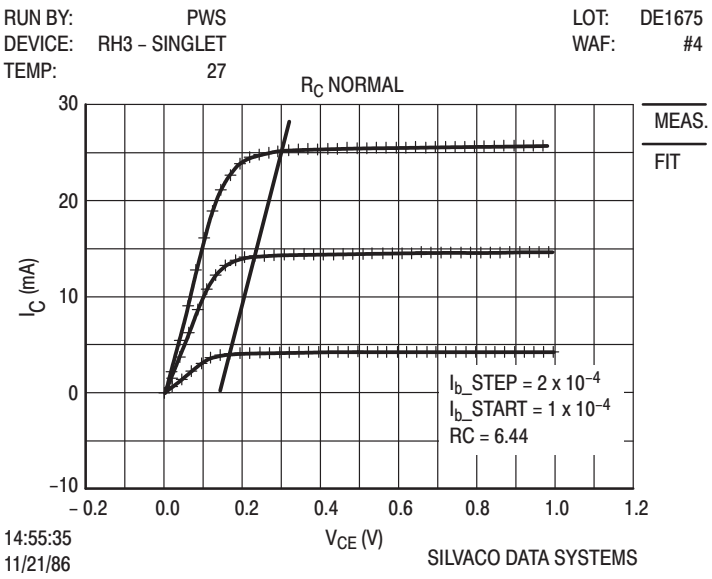

Figure 5. RC Extraction

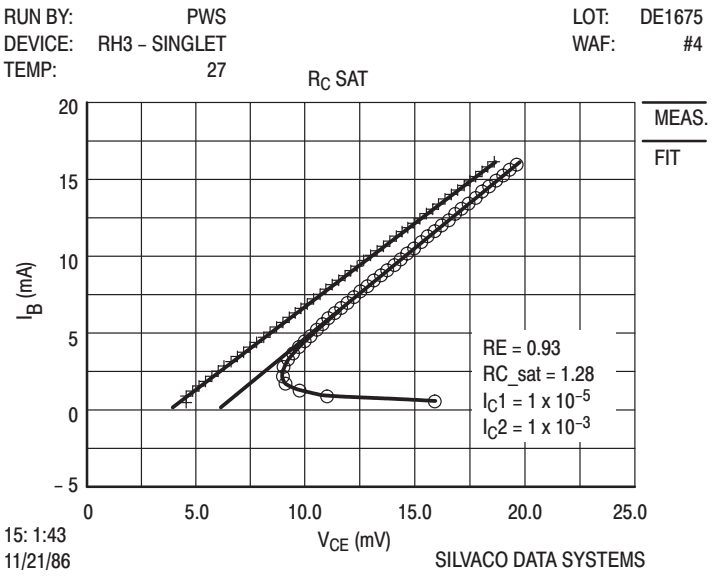

Figure 6. Flyback Measurement

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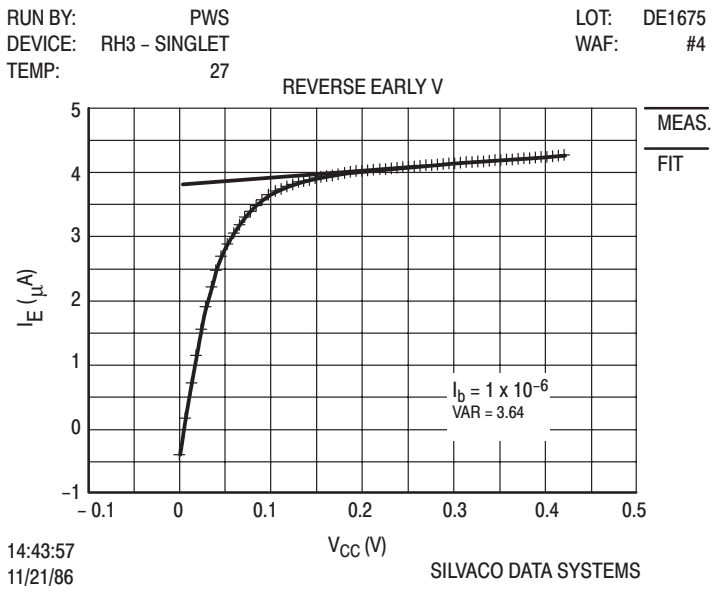

Figure 7. Reverse Early Voltage Plot

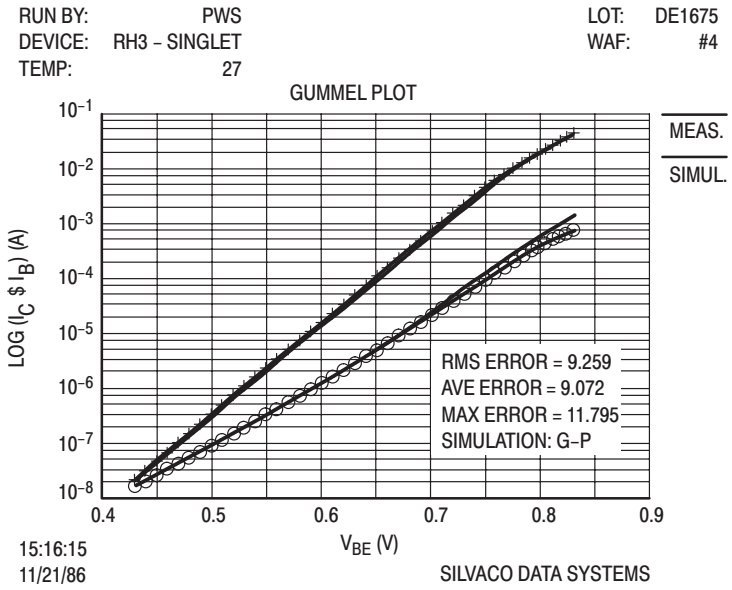

Figure 8. Simulated vs Measured Gummel Plot

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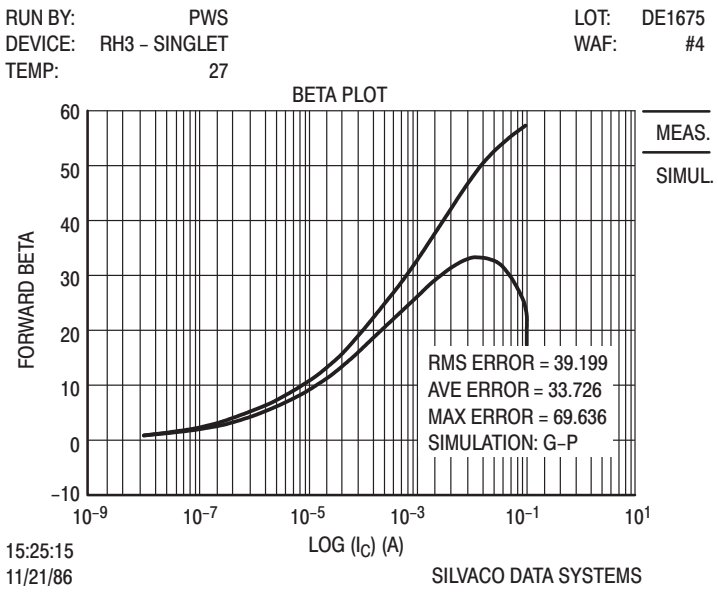

Figure 9. Simulated vs Measured Beta Plot

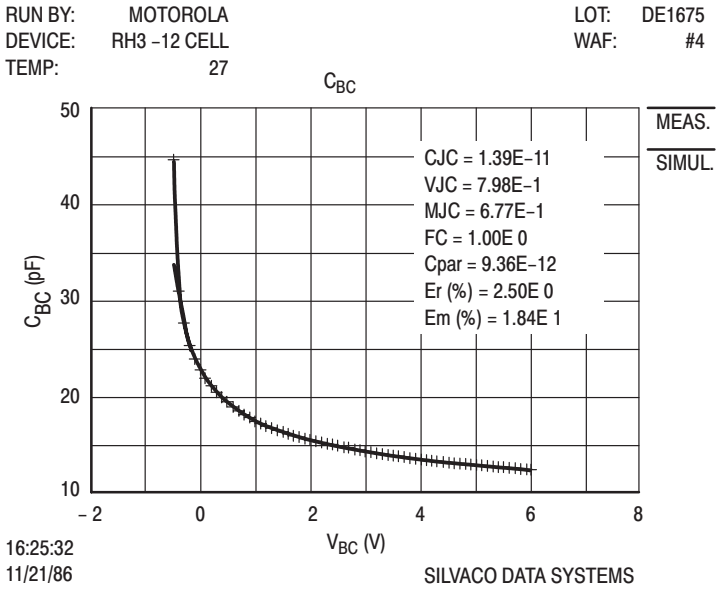

Figure 10. Simulated vs Measured CJC Plot

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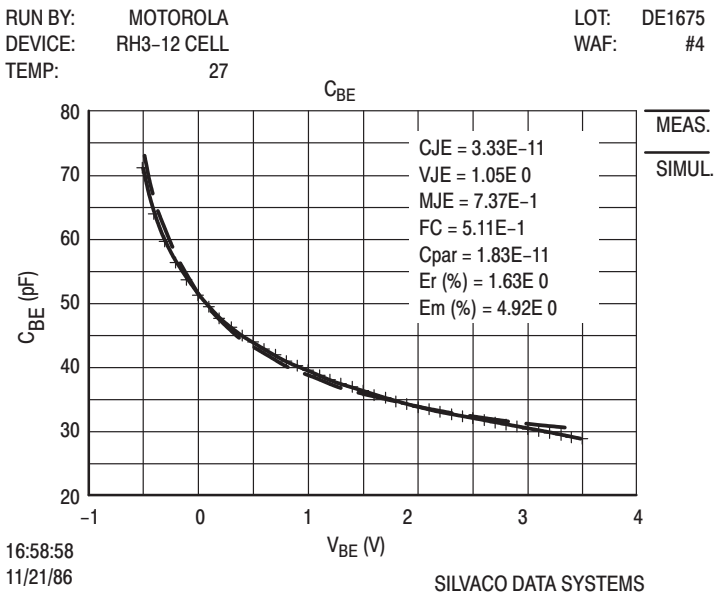

Figure 11. Simulated vs Measured CJE Plot

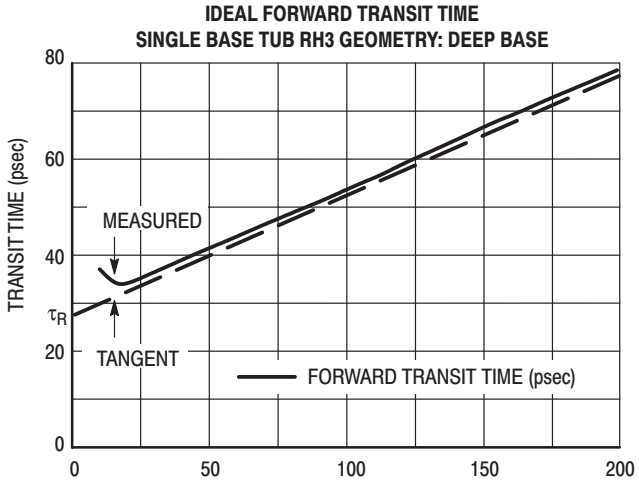

Figure 12. $I/(2\pi F_t)$ vs I/I_C Forward Plot

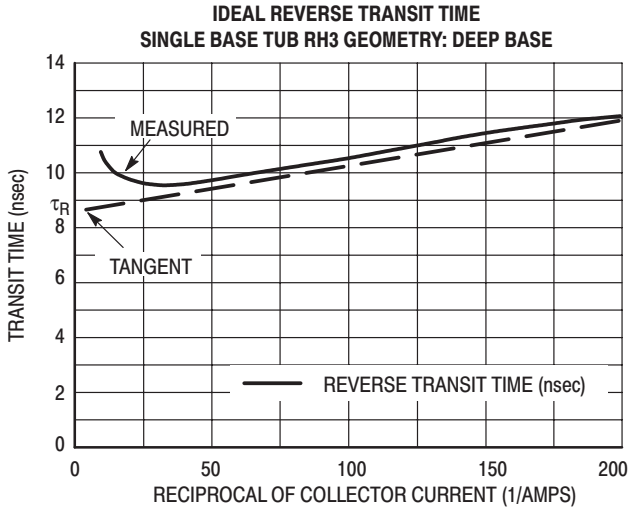

Figure 13. $I/(2\pi F_t)$ vs I/I_C Reverse Plot

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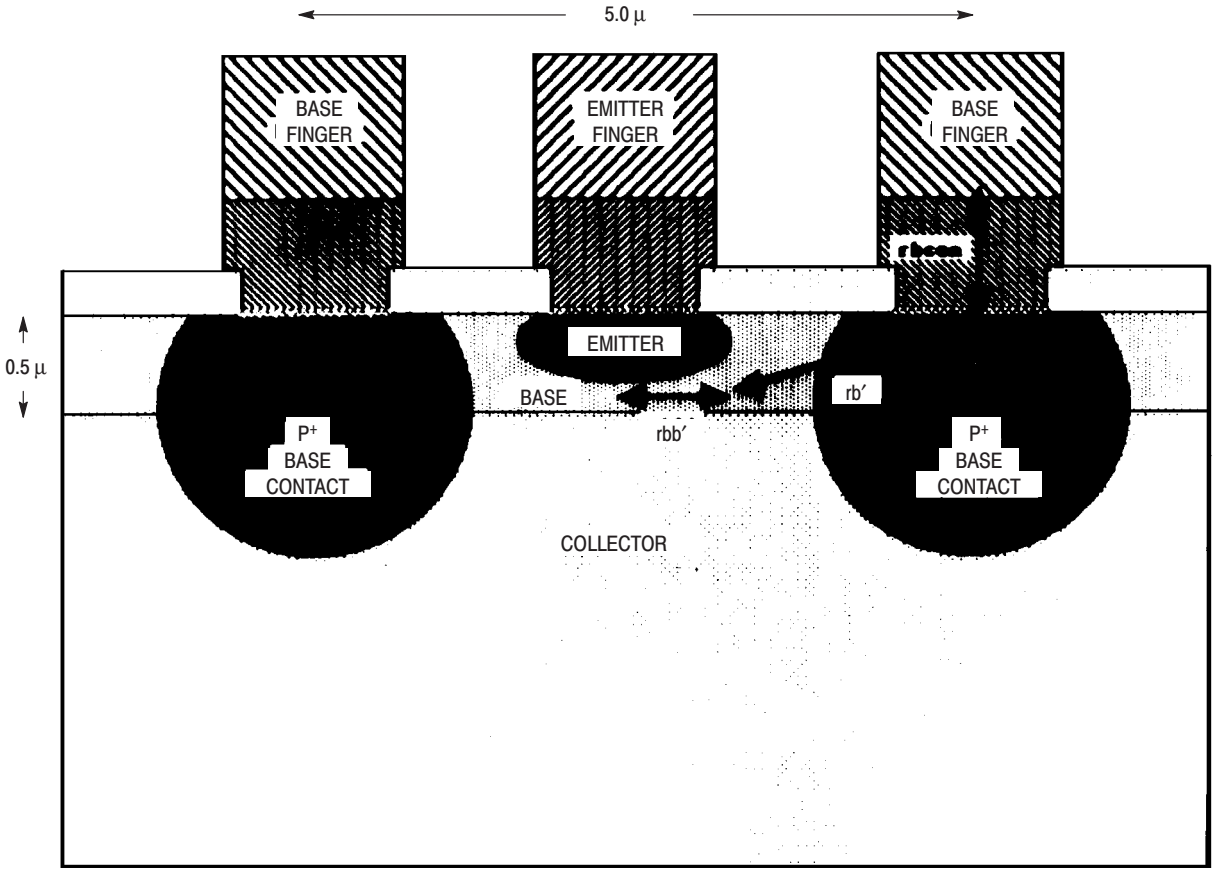

Figure 14. Cross Section Showing Major R_B Components

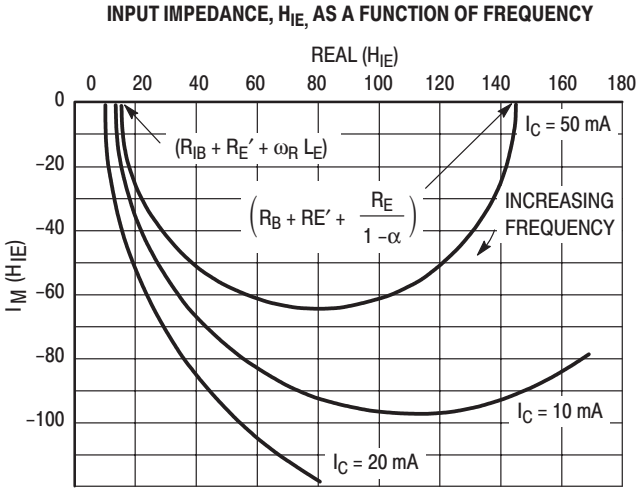

Figure 15. R_B, R_{BM}, and I_{RB} Extracted from Input Impedance Circles Plot

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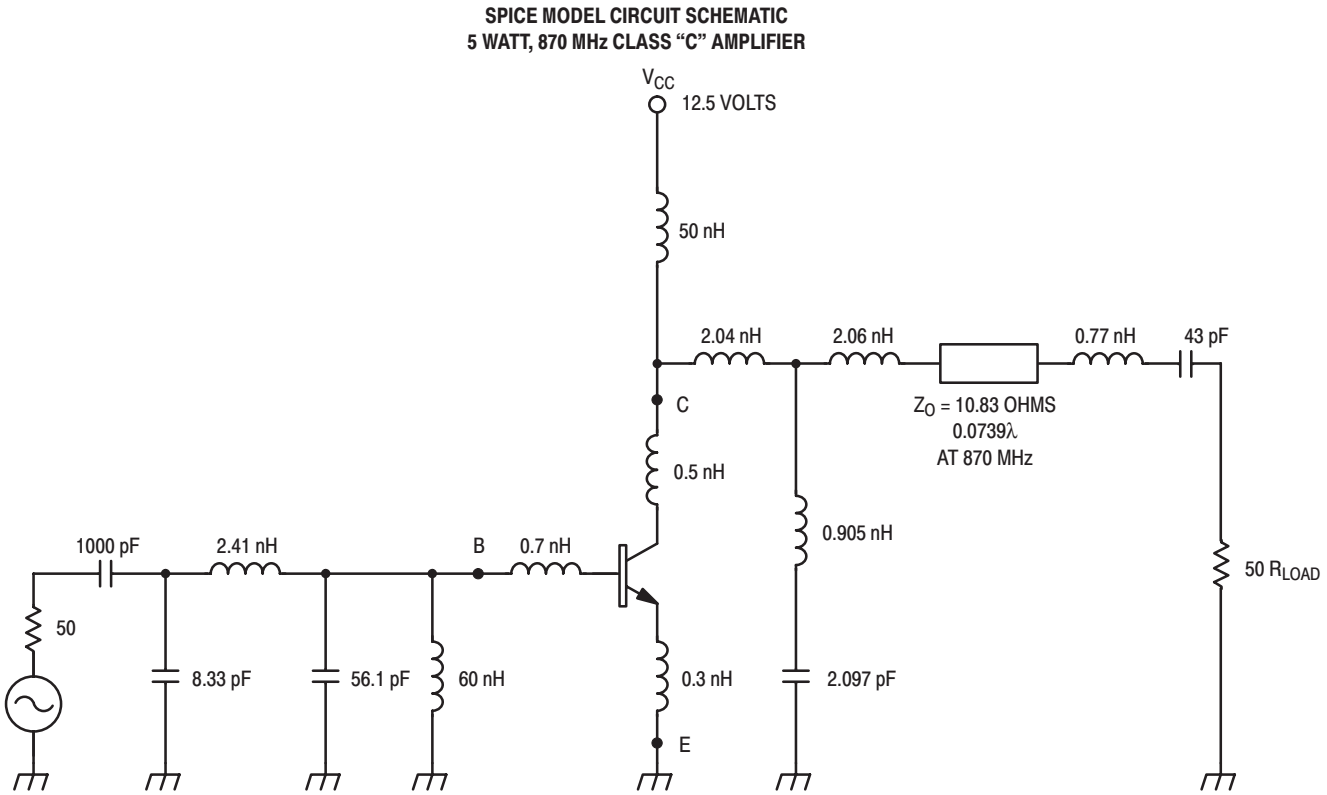

Figure 16. Amplifier Circuit Diagram

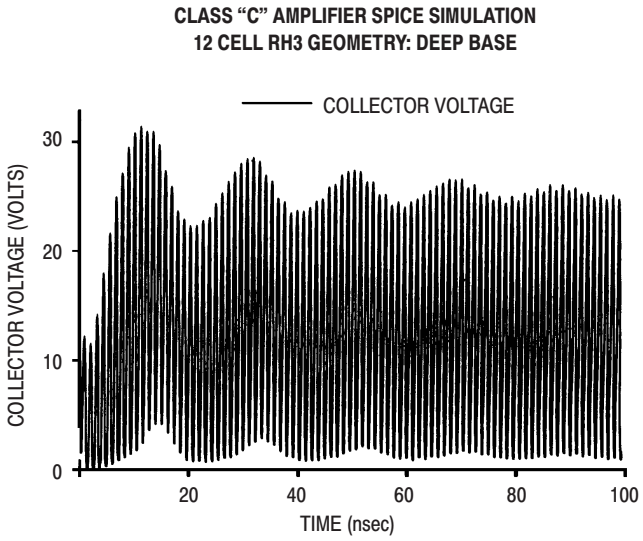

Figure 17. SPICE Output for Collector Waveform, Initial 100 ns

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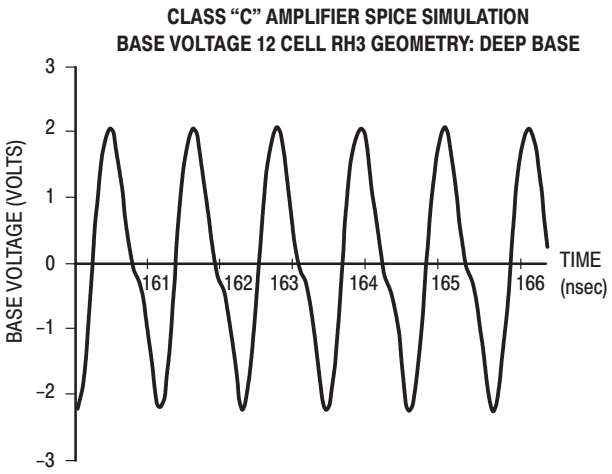

Figure 18. SPICE Output Expanded Plot of Base Voltage After 160 ns

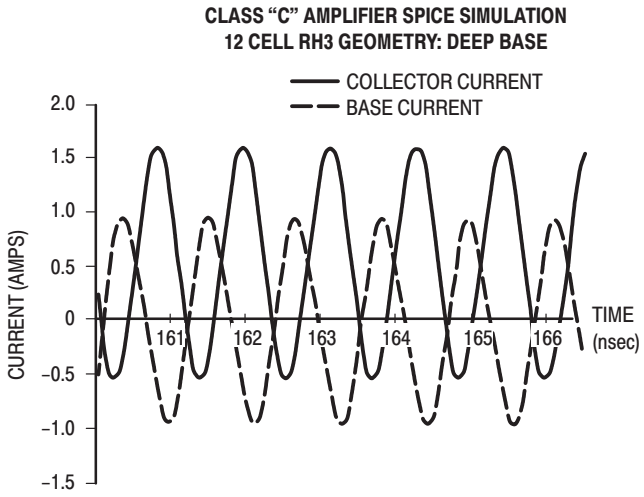

Figure 19. SPICE Output Expanded Plot of Collector and Base Current After 160 ns

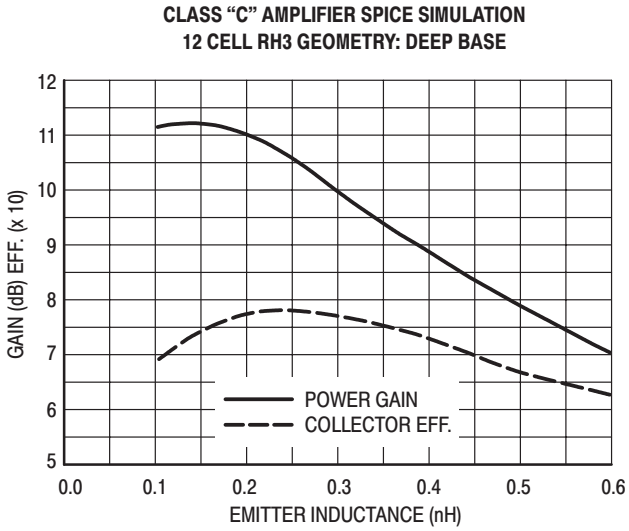

Figure 20. SPICE Output of Gain and Efficiency vs Emitter Inductance

```
CLASS 'C' AMPLIFIER (12 CELL RH3 UNMATCHED)
VCC  9  0  12.5
RS  1  22  50
VISM  22  2
CB1  2  3  1000PF
LBC1  4  0   60NH
CSHUNT1  3  0  8.328PF
CSHUNT2  4  0  56.12PF
LBIN1  3  4  2.41NH
LB   55  5  0.75NH
CEPARS  5  7  18.46PF
VIBM  4  55
LC   18  8   0.750NH
CCPARS  6  7  13.54PF
LE   7  0  0.30NH
VICM  18  6
LCC  8  9  40NH
LSER1  8  10  2.039NH
CCSHUNT  10  15  2.097PF
LCSHUNT  15  0  0.9046NH
LSER2  10  11  2.0592NH
RLOAD  14  0   50
TRL2  11  0  12  0  Z0=10.83  F=870MEG  NL=0.0739
CSER1  12  13  43PF
LCSER2  13  14  0.77NH
VIN  1  0  SIN(0  15  870MEG)
Q1  6  5  7  MOD1  AREA=12
.MODEL  MOD1  NPN (BF=64  IS=1.67E–15  NF=0.994  NR=0.946  BR=4.5
+                  ISE=4.56E–13  NE=1.5894  ISC=1.108E–15  NC=1.049
+                  VAF=16  VAR=10  IKF=0.42  IKR=0.042
+                  RB=2.70  RBM=0.67  IRB=0.014A
+                  CJE=3.05PF  MJE=0.767  VJE=1.2
+                  CJC=1.165PF  MJC=0.573  VJC=0.861
+                  RE=1.44  RC=10.8
+                  TF=0.028NS  XTF=6  ITF=0.29A  VTF=24
+                  TR=9.00NS  PTF=16)
.TRAN  0.05NS    123NS  120NS
.WIDTH  IN=80  OUT = 132
.OPTIONS  LIMPTS=2500  ITL5=50000
.FOUR  870MEG  V(14)
.PLOT  TRAN  V(2)  I(VISM)  V(4)  I(VIBM)  I(VCC)  V(6)
.END
```

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